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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/994,038	12/18/1997	SHUNPEI YAMAZAKI	07977/208001	6059

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EXAMINER	
COLEMAN, WILLIAM D	
ART UNIT	**PAPER NUMBER**
2823	

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05/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
08994038	December 18, 1997	YAMAZAKI ET AL.	07977/208001

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EXAMINER	
W. David Coleman	
ART UNIT	**PAPER**
2823	20060821

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

The Information Disclosure Statement filed January 29, 2003 has been considered.

W. David Coleman
Primary Examiner
Art Unit: 2823

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 08/994,038
Filing Date: December 18, 1997
Appellant(s): YAMAZAKI ET AL.

John F. Hayden
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed March 20, 2006 appealing from the Office action mailed September 30, 2004.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,873,003	Inoue et al.,	02-1999.
5,582,640	Okada et al.,	12-1996

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 1 03

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 2, 6, 12, 14, 16, 18, 19,12, 22, 23, 24, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue et al., U.S. Patent 5,873,003 in view of Okada et al., U.S. Patent 5,582,640.

3. Pertaining to claim 2, Inoue discloses a semiconductor device substantially as claimed. See FIGS. 1-50, where Inoue teaches a semiconductor device comprising:

a plurality of photodiodes 403 (as seen in FIG. 22) being formed in a matrix on an insulating surface 1609;

a plurality of vertical charge coupled devices on the insulating surface, said vertical charge coupled devices being connected with the plurality of photodiodes; (see FIG. 16);

at least a horizontal charge coupled device on the insulating surface, said horizontal charge coupled device being connected with the vertical charge coupled devices, wherein at least one of the vertical and horizontal charge coupled devices comprises a crystalline semiconductor film having a plurality of crystals extending in a crystal growth direction,

wherein a crystal structure of the crystalline semiconductor film 1753 in the crystal growth direction is continuous so that a charge moving is not restricted by a grain boundary.

However, Inoue fails to explicitly teach wherein at least one of the vertical and horizontal charge coupled devices that has the crystalline semiconductor film is arranged such that a charge transfer direction of the at least one of the vertical and horizontal charge coupled devices is coincident with the crystal growth direction. Okada teaches that the crystalline semiconductor film is arranged such that a charge transfer direction of the at least one of the vertical and horizontal charge coupled devices is coincident with the crystal growth direction. See FIGS. 1-158(h) where Okada teaches horizontally crystallization, also see FIG. 50(d) where Okada teaches the growth direction of the silicon grain. In view of Okada, it would have been obvious to the crystalline semiconductor film is arranged such that a charge transfer direction of the at least one of the vertical and horizontal charge coupled devices is coincident with the crystal growth direction, because the mobility between the presence and absence of the grain boundary becomes more remarkable (column 62, lines 34-56).

4. Pertaining to claim 23, Inoue discloses further an active matrix display device. Okada teaches a semiconductor device to be an active matrix display device. In view of Okada, it would have been obvious to one of ordinary skill in the art to incorporate the active matrix

display device of Okada into the Inoue device because a high quality picture is reproduced (column 1, lines 25-27).

5. Pertaining to claim 11, Inoue discloses wherein the crystalline semiconductor film 2 is formed over a quartz substrate, and wherein an incident light is made from a side of the quartz substrate (see claim 12 of Inoue).

6. Pertaining to claim 12, Inoue discloses wherein the charge transfer direction includes a plurality of directions (polycrystalline film option).

7. Pertaining to claim 14, Inoue discloses wherein the semiconductor film is a silicon film. Pertaining to claims 17 and 20, Inoue discloses wherein the crystalline semiconductor film is formed over a quartz substrate.

8. Pertaining to claims 16 and 19, Inoue discloses a semiconductor device comprising: a crystalline semiconductor film being formed on an insulating surface,

said crystalline semiconductor film having a plurality of crystals extending in a crystal growth direction (polycrystalline) which is parallel to the insulating surface;

an insulating film on the crystalline semiconductor film;

a plurality of electrodes being formed on the insulating film, each of said plurality of electrodes being located within a predetermined distance so that a plurality of MOS capacitors 11 formed between the plurality of electrodes and the crystalline semiconductor film with the insulating film therebetween,

wherein a charge transferred from one of the MOS capacitors to another of the MOS capacitors in a charge transfer direction,

wherein a crystal structure of the crystalline semiconductor film is continuous so that the crystal structure is regarded as single crystal for the charge,

wherein the charge transfer direction is coincident with said crystal growth direction.

9. Pertaining to claim 18, Inoue discloses wherein the semiconductor device consist of an image sensor.

10. Pertaining to claims 21 and 22, Inoue discloses an image sensor (CCD), which consist of a photodiode.

11. Pertaining to claims 25 and 26, Inoue discloses a semiconductor device comprising:

a photoelectric conversion (silicon interacting with light) formed over an insulating surface;

a charge coupled device electrically connected to the photoelectric conversion device and formed over the insulating surface;

said charge coupled device including:

a crystalline semiconductor film formed on the insulating surface, said crystalline semiconductor film having a plurality of crystals (polycrystalline silicon as taught by Inoue) extending in a crystal growth direction which is parallel to the insulating surface;

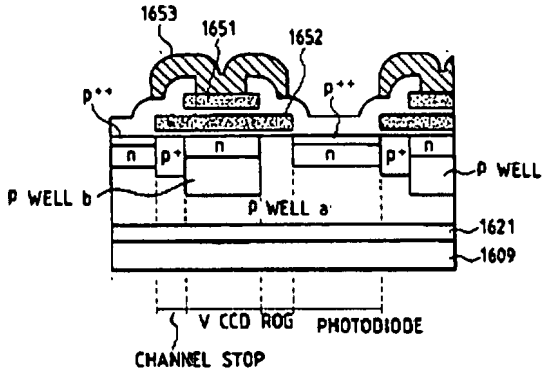
an insulating film on the crystalline semiconductor film (MOSFET section);

a plurality of electrodes (having a predetermined distance, which becomes an active matrix display) formed on the insulating film (Inoue teaches forming an array, column 6, lines 8-11) so that a plurality of MOS capacitors are formed between the plurality of electrodes and the crystalline semiconductor film with the insulating film therebetween,

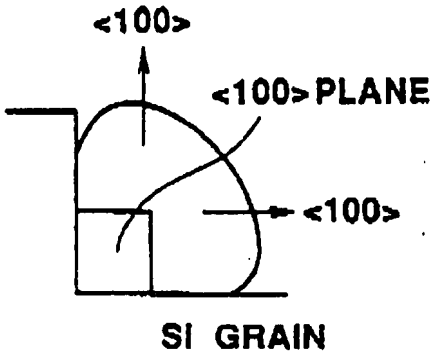
wherein a charge is transferred from one of the MOS capacitors to another of the MOS capacitors in a charge transfer direction,

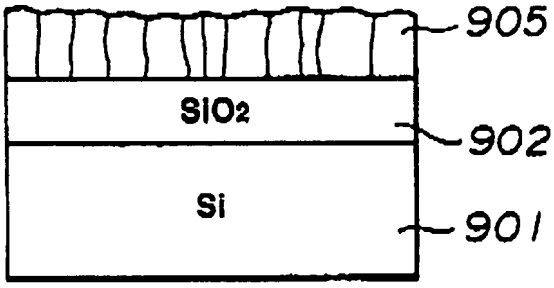
wherein the charge transfer direction is coincident with the crystal growth direction.

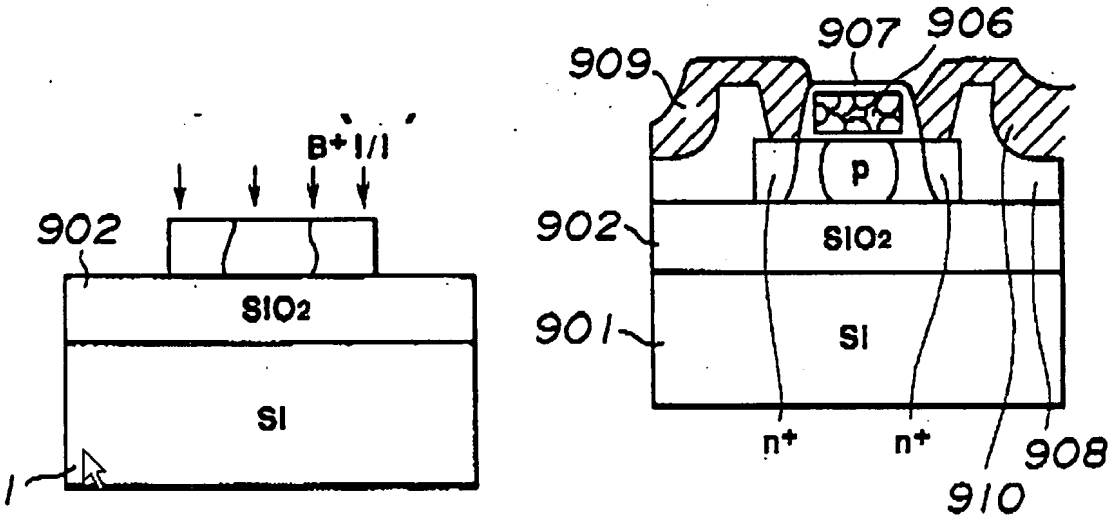
Inoue teaches a plurality of photodiodes, see FIG. 50 and that the thin film transistors (i.e., MOSFETS can be single crystal (see column 3, line 48)



Okada teaches the structure of a typical MOFSET which is used as a photodiode, see FIGS. 84(a)-84(g) discloses a single crystal silicon wherein the crystal structure of the crystalline semiconductor film 905 in the crystal growth direction is continuous so that a charge moving is not restricted by a grain boundary.







(10) Response to Argument

Applicants contend that the combined teachings fail to disclose at least one vertical and one horizontal charge coupled device having a plurality of crystals extending in a crystal growth direction.

Although the primary reference does not explicitly teach the crystal growth direction coinciding with the charge transfer direction, the primary reference does teach that the material can be polycrystalline silicon or single crystalline silicon are semiconductors and therefore Applicants argument is moot. All polycrystalline semiconductor materials and single crystal semiconductor materials deposited on a substrate will grow in a vertical direction (i.e. thickness) and a horizontal direction (width) and all materials have at least two (2) dimensions and thickness and width being at least two of three (3) dimensions. Since the primary reference teaches polycrystalline silicon and single crystalline silicon, charge traveling along the crystal is only limited by the grain boundary. Applicants have failed to disclose why the charge moving (i.e., electrons) along the grain boundary of the crystal is different from the prior art. One of the

major reasons why there is charge traveling in the semiconductor material is because impurities such as phosphorus, arsenic or boron is introduced into the semiconductor material. Applicants disclosure is silent as to why the material as claimed is different from the prior art material. All materials of the same substance and same structure will have the same properties and the Applicants have failed to distinguish any differences.

Applicants contend that the claims are allowable because the term "a crystal structure of the crystalline semiconductor film in the crystal growth direction is continuous so that a charge moving is not restricted by a grain boundary" is a unique feature.

In response to Applicants contention that the term "a crystal structure of the crystalline semiconductor film in the crystal growth direction is continuous so that a charge moving is not restricted by a grain boundary" is a unique feature, please note that the claimed limitations are obvious features of semiconductor materials that have the same crystal structure, and therefore Applicants argument is moot. It is well known that charge traveling through or along amorphous material has reduced mobility since the path or distance of the charge traveling is increased (i.e., various paths to move from point A to point B), mobility has a relationship with resistance. Polycrystalline semiconductor material has increased mobility as compared to amorphous semiconductor material and single crystal semiconductor material has increased mobility as compared to polycrystalline semiconductor material.

Applicants contend that the claims are allowable because the secondary reference is silent as to the term "CCD" (i.e., charge coupled device).

In response to Applicants contention that the secondary reference fails to disclose the term "CCD", the secondary reference was relied upon only for the structure of the crystalline

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

(12) Evidence Appendix

There are no affidavits, transcripts of depositions or documents submitted as exhibits in the Appeal Brief.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Conferees:

Matthew Smith, Supervisory Primary Examiner (SPE)

MATTHEW SMITH
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TECHNOLOGY CENTER 2800

Daren Schulberg, Supervisory Primary Examiner (SPE)

W. David Coleman, Primary Examiner (PE)

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCE

Ex parte SHUNPEI YAMAZAKI and SATOSHI TERAMOTO

Application 08/994,038

ORDER RETURNING UNDOCKETED APPEAL TO EXAMINER

This application was electronically received at the Board of Patent Appeals and Interferences (BPAI) on August 28, 2006. A review of the application has revealed that the application is not ready for docketing as an appeal. Accordingly, the application is herewith being returned to the examiner. The matters requiring attention prior to docketing are identified below.

Information Disclosure Statement (IDS) were filed January 29, 2003. It is not clear from the record whether the examiner considered the IDS or whether the examiner notified appellants of why their submission did not meet the criteria set forth in 37 CFR §§ 1.97 and 1.98.

A review of the file indicates that on March 20, 2006, appellants filed an Appeal Brief under the rules set forth in 37 CFR § 41.37(c). However, the Appeal Brief filed on March 20, 2006, does not fully comply with the new rules under 37 CFR § 41.37(c).

37 CFR § 41.37(c) states in part:

> (c)(1) The brief shall contain the following items under appropriate headings and in the order indicated in paragraphs (c)(1)(I) through (c)(1)(x) of this section, except that a brief filed by an appellant who is not represented by a registered practitioner need only substantially comply with paragraphs (c)(1)(I) through (c)(1)(iv) and (c)(1)(vii) through (c)(1)(x) of this section:
>
> > (ix) ***Evidence appendix***. An appendix containing copies of any evidence submitted pursuant to §§ 1.130, 1.131, 1.132 of this title or of any other evidence entered by the examiner and relied upon by appellant in the appeal, along with a statement setting forth where in the record that evidence was entered in the record by the examiner. Reference to unentered evidence is not permitted in the brief. See § 41.33 for treatment of evidence submitted after appeal. This appendix may also include copies of the evidence relied upon by the examiner as to grounds of rejection to be reviewed on appeal.

An in-depth review of the Appeal Brief indicates that the following sections are missing from the Appeal Brief filed March 20, 2006:

1) "Evidence Appendix," as set forth in 37 CFR § 41.37(c)(1)(ix).

It is required that a supplemental Appeal Brief be submitted that is in compliance with 37 CFR § 41.37(c). For more information on the Board's new rules, please see the web page entitled "More Information on the Rules of Practice Before the BPAI," Final Rule at:

http://www.uspto.gov/web/offices/dcom/bpai/fr2004/moreinfo.html.

On April 21, 2006, an Examiner's Answer was mailed. A review of the Examiner's Answer reveals that it is not in compliance with the headings as required under 37 CFR § 41.37(c).

An in-depth review of the Examiner's Answer mailed on April 21, 2006, reveals that under the heading Evidence Relied Upon, the prior art relied on was not listed. The MPEP 1207.02(A) states:

> A) CONTENT REQUIREMENTS FOR EXAMINER'S ANSWER. The examiner's answer is required to include, under appropriate headings, in the order indicated, the following items:
>
> > (8) *Evidence Relied Upon.* A listing of the evidence relied on (e.g., patents, publications, admitted prior art), and, in the case of nonpatent references, the relevant page or pages.

Proper correction of the Examiner's Answer is required.

Accordingly, it is ORDERED that the application is return to the Examiner:

1) to consider the Information Disclosure Statement filed January 29, 2003;

2) provide appropriate written notification by the examiner to appellants of such consideration; and

3) hold the Appeal Brief filed on March 20, 2006, defective;

4) notify appellants to file a supplemental Appeal Brief in compliance with 37 CFR § 41.37 or for the examiner to present a statement regarding the position taken on the missing appendices;

5) if necessary, vacate the Examiner's Answer mailed April 21, 2006, and issue a revised Examiner's Answer in response to the supplemental Appeal Brief;

6) issue a revised Examiner's Answer, setting forth the prior art the Examiner used in the rejections on appeal; and

6) for such further action as may be appropriate.

BOARD OF PATENT APPEALS
AND INTERFERENCES

DALE M. SHAW
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Application 08/994,038

DMS/pgc

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